crystal oscillator provides an output signal at a predetermined frequency which is used for tuning the analog front end **108**. However, the output frequency of the crystal oscillator varies with factors such as temperature and aging. This can lead to inaccuracies in tuning, so techniques have been developed to compensate for the variation. One example is by synchronizing to a received signal having a known frequency, for example from base station **102**, after communication has begun between the radiotelephone **104** and the base station **102**. Before CDMA system acquisition, the receiver **104** has only the frequency accuracy of its crystal oscillator. This accuracy is typically 2.5 parts per million; including both temperature and aging variation. At 900 MHz for example, he maximum frequency offset is 2250 Hz. This accuracy may cause a frequency offset between the tuned reception frequency at the radiotelephone **104** and the transmitted frequency at the base station **102**.

Frequency offset causes a phase rotation of the modulation at a rate equal to the frequency offset. One hundred eighty degrees of phase rotation will turn a chip transmitted with a value of +1 into a chip received with a value of −1. Thus, when summing chips in the prior art searching method or when using a matched filter, there is a practical limit to the number of sequential chips that can be summed and matched.

With a 2250 Hz frequency offset, a phase rotation of 90 degrees will occur in 111.1 microseconds. A chip in an IS-95 based system has a time length of 0.8138 microseconds. Thus, 136.5 chip times occur in 111.1 microseconds, so 136 chips could be safely summed or matched while maintaining phase coherence.

If 512 chips are to be matched, then the maximum frequency offset for 90 degrees of phase rotation is 600 Hz. This requirement is easily met after CDMA system acquisition and locking of the tuning frequency of the receiver **104** to the base station's transmission frequency. However, before system acquisition, to obtain the match response accuracy of 512 chips with greater than 600 Hz of frequency offset, other provisions are necessary.

In FIG. **5**, I filter **140** comprises multiple matched filters, including matched filter **502**, matched filter **504**, matched filter **506** and matched filter **508**. Similarly, Q filter **142** comprises multiple matched filters, including matched filter **510**, matched filter **514**, matched filter **516** and matched filter **518**. The first matched filter in each set, matched filter **502** of I filter **140** and matched filter **510** of Q filter **142**, has an input coupled to the ADC **110** for receiving the I PN sequence and the Q PN sequence, respectively. Subsequent matched filters in each set each have an input coupled to an output of the previous matched filter to receive the detected PN sequence at a subsequent time for matching.

Each matched filter compares a portion of the detected PN sequence and a predetermined PN sequence and produces a respective response. Each matched filter has a respective output coupled to a summing element **520**. The summing element **520** combines the respective filter responses to produce a total response. The total response is stored in the memory **522**.

In the illustrated embodiment, the I filter **140** and the Q filter **142** each comprise four matched filters. Any number of matched filters could, of course, be provided, depending of acceptable levels of hardware complexity, the number of chips to be matched, and other factors. If four matched filters are provided and 512 chips are to be matched, the first-received 128 chips of the detected I PN sequence are matched in matched filter **508**, the second-received 128 chips of the I PN sequence are matched in matched filter **506**, the third-received 128 chips of the I PN sequence are matched in matched filter **504**, and the last-received 128 chips of the I PN sequence are matched in the matched filter **502**. Similarly, for the Q PN sequence, the first-received 128 chips of the detected Q PN sequence are matched in matched filter **518**, the second-received 128 chips of the Q PN sequence are matched in matched filter **516**, the third-received 128 chips of the Q PN sequence are matched in matched filter **514**, and the last-received 128 chips of the Q PN sequence are matched in the matched filter **510**. Received chips are clocked sequentially through the matched filters using, for example, the chip clock signal. At each clock time, the summing element **520** provides the response to the memory **522**. Thus, the matched filter is split into multiple matched filters with short chip match lengths to obtain match response accuracy of 512 chips in the presence of frequency offset greater than 600 Hz.

A second alternative embodiment for maintaining the match response accuracy of, for example, 512 chips in the presence of excessive frequency offset is the use of shorter chip length matched filters whose outputs from successive 26⅔ milliseconds PN sequence times are combined. For example, referring again to the embodiment illustrated in FIG. **1**, to match 512 chips using this alternative embodiment, each of I filter **140** and Q filter **142** is 128 chips in length. During a first 26⅔ milliseconds PN sequence time, a first 128 chips are matched by each filter and the response stored. During a second 26⅔ milliseconds PN sequence time, a second 128 chips are matched by each filter and the response stored or combined with the first response. A third and a fourth 128 chips are subsequently matched and the responses combined with the first and second responses to produce the total response. Thus, the matched filter combines the response from a predetermined number of successive matches to produce the total response.

The second alternative embodiment provides similar accuracy to the accuracy of the embodiment illustrated in FIG. **5**. The second alternative embodiment provides for reduced hardware complexity, but matching takes approximately four times as long, or 4×26⅔ milliseconds=106⅔ milliseconds. This performance is still satisfactory during the initial process of CDMA system acquisition.

As can be seen from the foregoing, the present invention provides method and apparatus for fast pilot channel acquisition using a matched filter in a mobile station. The receiver searcher **114** includes a matched filter **128** for comparing detected PN sequences with a predetermined PN sequence and storing the result of the comparison. The comparison may be completed every 26⅔ ms, corresponding to the repetition rate of the base station PN sequences for the I and Q channels. The comparison is repeated continuously, independent of other processes in the mobile station. Using this process, CDMA energy may be reliably detected within the 26⅔ ms search time and receiver fingers assigned, greatly reducing the search time required by conventional receiver searchers. The process also improves performance of the mobile station during idle mode handoff, slotted mode operation and soft handoff by reducing the pilot channel search time.

While a particular embodiment of the present invention has been shown and described, modifications may be made. It is therefore intended in the appended claims to cover all such changes and modifications which fall within the true spirit and scope of the invention.

What is claimed is:

1. A radiotelephone configured to receive DS-CDMA signals in a communication system including a plurality of